REMARKS

Status of the Claims

Claim 1 is currently present in the Application, and claim 1 is an independent claim. Claim 1 has been amended, no claims have been canceled, and no claims have been added in this response.

Applicants are not conceding that the subject matter encompassed by claims 1-47, prior to this and previous amendments, are not patentable over the art cited by the Examiner. Claim 1 was amended in this amendment solely to facilitate expeditious prosecution of this Application. Applicants respectfully reserve the right to pursue claims, including the subject matter encompassed by claims 1-47 as presented prior to this and previous amendments, and additional claims in one or more continuing applications.

Examiner Interview

Applicants note with appreciation the telephonic interview conducted between Applicants' representative and the Examiner on June 26, 2008. During the telephonic interview, the Examiner and Applicants' representative discussed one of the 103 references (Bono, U.S. Patent Pub. 2003/0018691). In particular, Applicants' representative discussed that Applicants' first processor loads data and an instruction block, and sends a message to a second processor that includes the location of the instruction block. In contrast, Bono's first processor stores processor threads in a queue that Bono's second processor retrieves and processes. Applicants' representative and the Examiner discussed a proposed amendment that further describes Applicants' novelty. The Examiner suggested that such amendment may read over the art of record but wished to review the prior art in more detail. No agreement was reached regarding the claims.

Drawings

Applicants note that the Examiner did not indicate whether the formal drawings, filed with Applicants' application, are accepted by the Examiner. Applicants respectfully request that the Examiner indicate whether the formal drawings are accepted in the next office communication.

Information Disclosure Statement

Applicants note that the Examiner has not reviewed the original Information Disclosure Statement filed with Applicants' application, and did not initial Applicants' "AN" reference on Applicants' Information Disclosure Statement mailed on March 29, 2007, which is a publication by Stallman. Applicants request the Examiner consider these references and send a copy of initialed form PTO-1449 for each IDS to Applicants.

Claim Objections Under 35 U.S.C. § 112

Claim 1 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. Applicants have amended claim 1 in this response and request removal of the 112 rejection to claim 1 in the next Office communication.

Provisional Claim Rejections – Nonstatutory Double Patenting

Claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending application number 10/670,838.

In order to expedite the allowance of Applicants' application, Applicants' attorney has included a terminal disclaimer with this response in compliance with 37 CFR 3.73(b), and request removal of the provisional double patenting rejection.

Claim Rejections – Alleged Obviousness Under 35 U.S.C. § 103

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bono (U.S. Patent Pub. 2003/0018691, hereinafter "Bono") in view of Wenkata

Subramanian et al. (U.S. Patent Pub. 2006/0047754, hereinafter "Wenkata"). Applicants respectfully traverse these rejections.

Applicants have amended independent claim 1 to distinctly claim steps of Applicants' first processor loading data and an instruction block into particular memory locations, and sending a message to a second processor that includes the location of the instruction block. Support for such amendment may be found in Applicants' specification on page 46, line 25 through page 49, line 7. Therefore, no new matter is added with such amendment. As amended, claim 1 is directed to a method with limitations comprising:

- loading data from a first processor to a first location in a common memory in a computer system;
- loading software code that processes the data in a second location in the common memory;
- writing an instruction block from the first processor to a third location in the common memory, wherein the instruction block includes the first and second locations;
- sending a message from the first processor to a second processor that includes the third location, the second processor included in a plurality of processors included in the computer system, wherein the plurality of processors share the common memory, wherein each of the processors have a local memory, and wherein at least two of the processors are dislike and heterogeneous;
- in response to receiving the message, retrieving, by the second processor, the instruction block from the third location;
- in response to retrieving the instruction block from the third location, copying, by the second processor, the data from the first location in the common memory to the second processor's local memory;
- in response to retrieving the instruction block from the third location, copying, by the second processor, the software code from the second location in the common memory to the second processor's local memory; and
- processing the data by the second processor using the software code stored in the second processor's local memory.

Applicants' first processor loads data into a first memory location and loads an instruction block into a third memory location. The instruction block includes the first

memory location and a second memory location in which device code is loaded. Next, Applicants' first processor sends a message to a second processor that includes the location of the instruction block and, in turn, Applicants' second processor retrieves the instruction block and subsequently retrieves data from the first location and processes the data with the device code stored in the second location.

In contrast, Bono discloses threads being stored in a queue, which are subsequently retrieved by a second processor to process. The Office Action points to an excerpt in Bono that states:

> "During execution time, in step 156, each processor executes a queue loader routine to load thread instances of its own program onto its own hard or soft affinity queue." (page 5, paragraph 86)

As can be seen from the above excerpt, Bono loads processor **threads** into a queue, which is not the same as "*loading **data** from a first processor to a first location in a common memory in a computer system*" as claimed by Applicants. The Office Action does not suggest that Wenkata teaches or suggests such limitations and, indeed, Wenkata does not teach such limitations.

In addition, Applicants' first processor writes an instruction block to a third location that includes the location of the data and program code. In contrast, Bono again loads processor threads into a queue that do not include both a first address for data and a second address for code. The Office Action points to an excerpt in Bono that states:

> "The memory contains memory-resident code threads, a queue loader routine for queuing code thread instances, a queue service routine for dispatching code thread instances to the processors for execution, and a code thread manager program using the queue loader routine." (page 2, para. 12)

As can be seen from the above excerpt, Bono uses a queue loader to distribute code threads, but does not teach or suggest "*writing an instruction block from the first processor to a third location in the common memory, wherein the instruction block **includes the first and second locations***" as claimed by Applicants. The Office Action

does not suggest that Wenkata teaches or suggests such limitations and, indeed, Wenkata does not teach such limitations.

Furthermore, Applicants' first processor and second processor are dislike, heterogeneous processors. In contrast, Bono's processors are homogeneous. Bono states:

> "The system includes multiple processors 21, 22, and 23, having respective processor numbers 0, 1, …, N-1, where N is the number of the processors. **The processors 21, 22, and 23, for example, are Intel PENTIUM (Trademark) processor chips**." (page 2, para. 28)

As can be seen from the above excerpt, although Bono teaches a multi-processor system, each of Bono's processors are the same. In addition, the Office Action states that Bono's processors "*may perform substantially different* ***functions***," page 4, 5th paragraph), which is not the same as teaching different types of **processors**. As such, Bono never teaches or suggests "*wherein at least two of the processors are* ***dislike and heterogeneous***" as claimed by Applicants. The Office Action does not suggest that Wenkata teaches or suggests such limitations and, indeed, Wenkata does not teach such limitations.

Therefore, since neither Bono nor Wenkata teach or suggest, either alone or in combination with each other, all the limitations included in claim 1 as amended, claim 1 is allowable over Bono in view of Wenkata.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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